Claims 1-21 have been rejected under 35 U.S.C.§ 103(a) as being unpatentable over the combination of Sandhu et al., U. S. Pat. No. 5,139,967 and Maeda et al., U. S. Pat. No. 5,314,538.

FORMAL MATTERS

Claims 1-21 have been rejected under 35 U.S.C.§ 112, second paragraph, with the Examiner objecting to the term "generally". In response, independent claims 1, 12 and 16 have been amended to address the Examiner's rejections, and thus claims 1-7 and 9-21 are now allowable with respect to 35 U.S.C.§ 112.

CLAIM REJECTIONS UNDER 35 U.S.C.§ 103(a)

Independent claim 1, as amended, provides a method for planarizing a BPSG layer deposited over a substrate. The method includes, *inter alia*, loading the substrate into a processing chamber, maintaining a temperature in the processing chamber between about 20 degrees Celsius and about 100 degrees Celsius, and exposing the substrate to an ultraviolet light. The ultraviolet light is at conditions sufficient to cause a reflow of the BPSG so that the upper surface includes a planar upper surface portion as a result of the reflow. In this manner, a UV light is used to help planarize a portion of the BPSG layer upper surface while maintaining a low temperature region in the substrate processing chamber. Advantages of the method of independent claim 1 are well identified in the present application, including, the reduction of the overall thermal budget associated with integrated circuit fabrication processes (see page 2, lines 22-27). The method as provided in amended independent claim 1 is neither disclosed, taught nor suggested by the cited art.

The cited reference Sandhu uses laser energy to attempt the reflow of a BPSG layer. Sandhu uses an intermittent pulse layer with pulses of approximately 25 nanoseconds. As recognized by the Examiner, Sandhu fails to disclose, teach or suggest the use of an ultraviolet light. Further, Sandhu fails to disclose, teach or suggest the problems attempted to be addressed by Applicants' invention, namely, the lowering of the

thermal budget used to process a substrate. Applicants' respectfully disagree with the Examiner's statement that wavelength is a routine optimization, in part since different effects may be produced on various materials depending on the electromagnetic energies used (i.e., ultraviolet, visible, infrared, radio, etc.).

The Examiner combines Sandhu with the Maeda reference, stating that Maeda discloses exposing a BPSG layer to ultraviolet radiation to densify the layer. However, the combination of Sandhu and Maeda also fails to disclose, teach or suggest the method provided in claim 1. First, Sandhu makes no mention of densifying or modifying the BPSG layer other than the attempted planarization thereof. Thus, there is no motivation within Sandhu to combine it with the Maeda reference, which, as the Examiner cites, attempts to use ultraviolet radiation to densify the BPSG layer.

Further, Maeda discusses two embodiments, both of which operate with substantially higher temperatures than provided in Applicants' claim 1. This again is not terribly surprising since Maeda has not recognized the problems Applicants are addressing, namely, the planarization of an insulating layer on a low thermal budget. For example, Maeda's second embodiment (discussed beginning on col. 8, line 60) attempts to use ultraviolet radiation to fill dangling bonds of the first $SiO_2$. Maeda maintains the substrate at a temperature of at least 400 degrees Celsius, including during the $SiO_2$ processing with UV. The BPSG layer reflow then is performed under an infrared lamp at a temperature of 800 degrees Celsius. Thus, this embodiment does not reflow with ultraviolet, but instead uses infrared wavelengths. The first Maeda embodiment (beginning on col. 4, line 42) also operates at significantly higher temperatures than is required by independent claim 1. The use of UV radiation occurs at a temperature of 400 degrees Celsius. Maeda fails to mention any specifics of the UV radiation energy or time necessary for the reflow.

Thus, for at least these reasons, Maeda, taken alone or in combination with Sandhu fails to disclose, teach or suggest Applicants' invention as provided in claim 1 which includes specific requirements as to the UV process. As a result, independent

claim 1 is allowable over the cited art. Claims 2-7 and 9-11 depend from independent claim 1 and are similarly allowable.

Independent claim 12 is allowable for at least the reasons described above. Again, Sandhu and/or Maeda taken alone or in combination, fail to disclose, teach or suggest the use of ultraviolet radiation at particular energy levels, for particular periods of time to cause a reflow of the insulating layer in a low thermal environment. Neither reference addresses the thermal constraints associated with advanced integrated circuit design. Further, as noted above, there is no teaching to combine Sandhu with Maeda, nor to practice either at lower temperatures. Thus, independent claim 12, and claims 13-15 which depend therefrom, are all in condition for allowance.

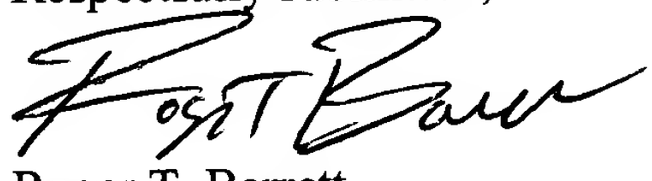
For at least the reasons described above in conjunction with independent claims 1 and 12, independent claim 16 is in condition for allowance. More specifically, independent claim 16 provides a method for forming a planarized insulating layer which includes, *inter alia*, exposing the layer to a UV light at conditions sufficient to cause the insulating layer reflow. Further, the substrate is maintained in a processing chamber at a temperature between 20 and 100 degrees Celsius during the UV light exposure. Thus, for at least these reasons, independent claim 16 is allowable over the cited art. Claims 17-21, and added claims 30-32 all depend from independent claim 16 and are similarly allowable.

## CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,



Roger T. Barrett
Reg. No. 41,599

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 303-571-4000
Fax: 303-571-4321

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

1. (Once amended herein) A method for planarizing a borophosphosilicate glass (BPSG) layer deposited over a substrate, said method comprising:

loading a substrate having a BPSG layer deposited thereover into a substrate processing chamber, said BPSG layer having **[an]** a non-planar upper surface **[that is generally non-planar]**;

cl. 8 maintaining a temperature in the substrate processing chamber between about 20 degrees Celsius and about 100 degrees Celsius; and

exposing said substrate to an ultraviolet (UV) light at conditions sufficient to cause a reflow of said BPSG so that said upper surface comprises a planar upper surface portion as a result of the reflow **[is generally planar]**.

2. (As filed) The method as in claim 1, further comprising producing said UV light with a UV lamp.

3. (As filed) The method as in claim 1, further comprising producing said UV light with a laser.

4. (As filed) The method as in claim 1, wherein said UV light has a wavelength of about 150 nm ± 50 nm.

5. (As filed) The method as in claim 1, wherein said UV light has an energy level that is greater than about 10 electron volts (eV).

6. (As filed) The method as in claim 1, wherein said UV light has an energy level that is about 15 eV.

7. (As filed) The method as in claim 1, wherein said exposing step has a duration that is between about thirty (30) seconds and about fifteen (15) minutes.

Please cancel claim 8.

9. (As filed) The method as in claim 1, wherein said exposing step comprises exposing said substrate to said UV light having a desired wavelength and a desired energy level to break at least some SiOH bonds in said BPSG layer.

10. (As filed) The method as in claim 1, wherein said exposing step densifies said BPSG layer.

11. (As filed) The method as in claim 1, wherein said BPSG layer comprises a premetal dielectric (PMD) layer.

12. (Once amended herein) A method for planarizing an insulating layer deposited over a substrate, said method comprising:

providing said substrate having said insulating layer deposited thereover;

providing a UV light source;

exposing said substrate to UV light from said UV light source; and

maintaining said UV light at an energy level that is at least about 10 eV for a duration that is at least about 30 seconds **[conditions sufficient]** to reflow said insulating layer to produce a **[generally]** planar portion of the insulating layer upper surface.

13. (As filed) The method as in claim 12, wherein said insulating layer comprises borophosphosilicate glass (BPSG).

14. (Once amended herein) The method as in claim 13, wherein said maintaining step comprises maintaining said UV light at an energy level that is at least

about 10 eV for a duration that is **[at least]** between about 30 seconds and about fifteen minutes to produce said reflow of said BPSG.

15. (As filed) The method as in claim 13, wherein said maintaining step comprises maintaining said UV light at a wavelength of about 150 nm and for a duration that is at least about 30 seconds.

16. (Once amended herein) A method of forming a planarized insulating layer, said method comprising:

providing a substrate having a non-planar upper surface;

depositing an insulating layer over said upper surface, said insulating layer having a **[generally]** non-planar upper surface; and

exposing said insulating layer to a UV light at conditions sufficient to cause said insulating layer to reflow so that said insulating layer upper surface comprises a planar upper surface portion **[is generally planar]**, wherein the substrate is maintained in a processing chamber at a temperature between about twenty (20) degrees Celsius and about one hundred (100) degrees Celsius during the exposing.

17. (As filed) The method as in claim 16, wherein said insulating layer comprises borophosphosilicate glass (BPSG).

18. (As filed) The method as in claim 17, wherein said depositing step comprises:

inserting said substrate into a substrate processing chamber; and

introducing a phosphorus-containing source and a boron-containing source into said processing chamber to deposit said BPSG insulating layer over said substrate.

19. (As filed) The method as in claim 16, wherein said UV light has an energy level that is at least about 10 eV.

20. (As filed) The method as in claim 16, further comprising performing said depositing and exposing steps in a substrate processing chamber.

21. (As filed) The method as in claim 16, further comprising performing said depositing step in a first processing chamber and said exposing step in a second processing chamber.

Please cancel claims 22-29.

Please add the following claims:

--30. The method as in claim 16 wherein the substrate non-planar upper surface comprises at least one trench having an aspect ratio of about 6:1, and wherein the reflow operates to fill the trench with the insulating layer.

31. The method as in claim 16 wherein the UV light has an energy level of at least about 15 eV.

32. The method as in claim 16 further comprising performing a chemical-mechanical polishing (CMP) process to the insulating layer upper surface after the exposing to further planarize the upper surface.--